

**EE 6330 – RFIC DESIGN**

**DESIGN OF LOW NOISE AMPLIFIER**

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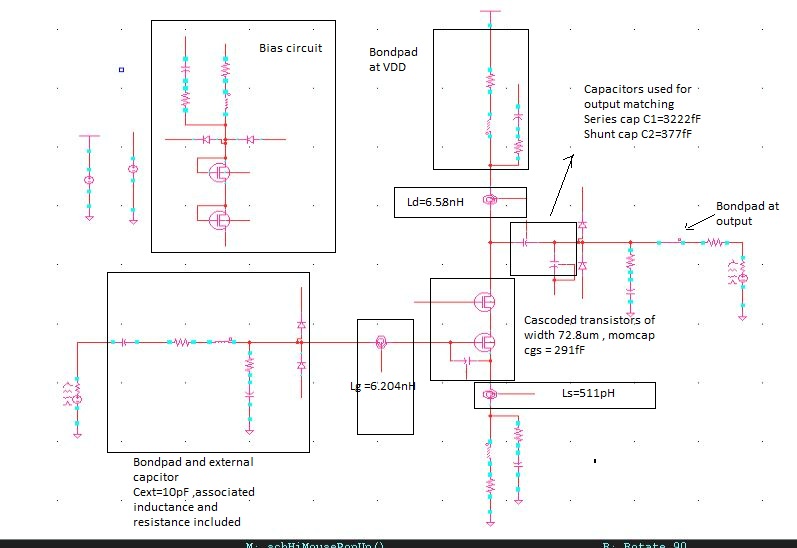
**Objective:**

The objective of this project is to design a low noise amplifier in 130nm technology with the following specifications:

* Operating Frequency : 2.4-2.5 GHz
* GT : > 12 dB
* Γin : Less than -10 dB
* Γout : Less than -10 dB
* VDD : 1.1 ~ 1.3 V
* IIP3 (input) : > -7 dBm
* Noise Figure (50 Ω) : < 2.0 dB

The operating frequency of the circuit shows that it is a narrow band amplifier. Hence while designing the circuit, we try to tune the components to the center frequency of operation ie 2.45GHz. To realize the amplifier, we go for a cascade topology due to high gain and better noise performance

**Circuit Description**

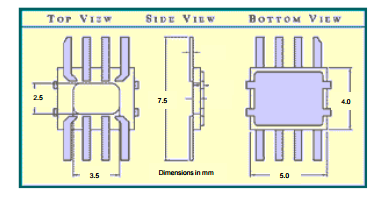
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The figure shows the circuit diagram used for simulation. The basic LNA circuit consists of the common source and common gate amplifiers, along with inductances at the source, gate and drain terminals. For the sake of simulations we have added the equivalent RLC network to account for package parasitics.

Since it is essential to protect the device from ESD events, we add back to back connected diodes as ESD dischargers at the pins. To achieve input matching and desired Qin, we connect a compensation capacitor between gate and source terminals. An additional external capacitor is required at the input to ensure correct operation. For the output matching between Ld and package parasitics, we use two capacitances – one in series, and the other in shunt.

To reduce the inductance at the lead, we add two ground pads so that the inductances appear in parallel.

**Package parasitics for simulation:**



The 8 pin package we assume has a width of 2.5mm. We estimate our chip area to be around 0.5mm X 0.5 mm. Based on this we assume the distance between the chip and the die to be around 1mm.

The bond wire length is estimated as follows:

X=1mm

L= (250-3.14) \*e-6 + x – 500\*e-6 = 0.74mm

On an average assume L= 1mm

Inductance of bond wire = 0.82pH/ um \* 1mm = 0.82nH

Inductance of lead = 1nH

Total inductance due to package parasistics = 0.82 + 1 = 1.82nh

At the input, we add an external cap which has a series inductance of 0.6Nh. This is added to the total parasitic inductance at the input. The inductance at the source is halved due to inductances appearing in parallel.

**Initial Hand and Matlab Analysis of the Circuit**

We use a Q based analysis to decide on the component values. In order to find Lg and Ls, we fix the value Qin using IIp3 specification of -7dbm.

%Qin calculation  
Zo=50;  
IIP3\_dbm=-7;  
IIP3\_lin=(10^(IIP3\_dbm/10)\*10^(-3));  
Vin=sqrt(IIP3\_lin\*2\*Zo);  
Vov=0.2;  
theta=1;  
syms Qin;  
value\_Qin=vpa(solve(Vin==(1/(2\*Qin))\*sqrt((8\*Vov)/(3\*theta)),Qin));  
disp(value\_Qin);

So, Qin should be less than 2.58. We choose Qin to be 1.7.   
In order to get a better Rs, we fix a big inductor size such that Ld= 5.7nH. Our initial simulations on “ind” shows that it has a Ql of 11.7 .We choose a gm such the transducer gain is pretty high than required value.

%%GT calculation  
gm1=25e-3;  
L= 5.79e-9;  
QL = 11.7;Zo=50;  
Fo=2.45e+9;  
Wo = 2\*pi\*Fo;  
Qin = 1.7;Rg1=1;  
syms GT;  
value\_GT= vpa(abs(solve((GT==(gm1)^2\*(Qin)^2\*L\*Wo\*Zo\*QL),GT)));  
GT\_db=10\*log10(value\_GT);  
disp(GT\_db);

GT(dB)=19.73

Fixing Qin also helps us fix initial values of Lg and Ls. While calculating Ls, we allocate gate resistance Rg to be 1 Ohm

%Lg calculation  
GT\_db = 19.74;  
Gt = 10^((GT\_db)/10);  
L= 5.79e-9;  
QL = 11.7;Zo=50;  
Fo=2.45e+9;  
Wo = 2\*pi\*Fo;  
Qin = 1.7;Rg1=1;  
gm1=25e-3;syms Lg;  
value\_Lg=vpa(abs(solve(Lg==((Qin\*2\*Zo)/Wo),Lg)));  
value\_ls1=(value\_Lg/(1e-9));  
disp(value\_ls1);

Lg = 11.043n

%Ls calculation  
GT\_db = 19.4;  
Gt = 10^((GT\_db)/10);  
L= 5.79e-9;  
QL = 11.7;Zo=50;  
Fo=2.45e+9;  
Wo = 2\*pi\*Fo;  
Qin = 1.7;Rg1=1;  
gm1=25e-3;  
syms Ls;  
value\_Ls=vpa(abs(solve(Ls==((Zo-Rg1)/(gm1\*(Qin)\*Wo\*2\*Zo)),Ls)));  
value\_ls1=(value\_Ls/(1e-9));  
disp(value\_ls1);

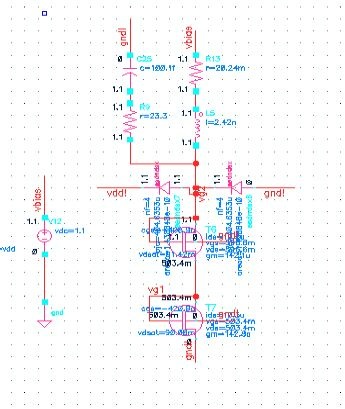
Ls = 0.748n

%Ct calculation  
Zo=50;  
Fo=2.45e+9;  
Wo = 2\*pi\*Fo;  
Qin = 1.7;  
syms Ct;  
value\_Ct=vpa(solve(Qin==(Wo\*Ct\*2\*Zo)^(-1),Ct));  
value\_Ct1=(value\_Ct/(1e-12));  
disp(value\_Ct1);

Ct = 0.38fF

**Bias Circuit:**

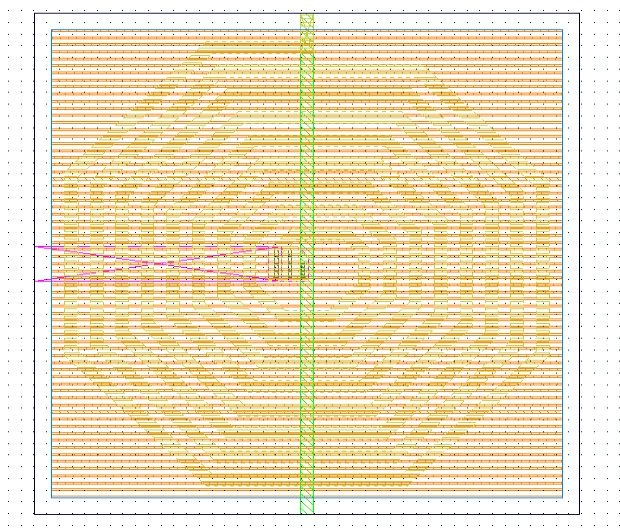
In order to properly bias the circuit we need to set the values of vg1 and vg2 to 0.5 V and 1V respectively. An external Vbias of 1.1 V is used and nfets are configured as a diode to give the required voltage values.

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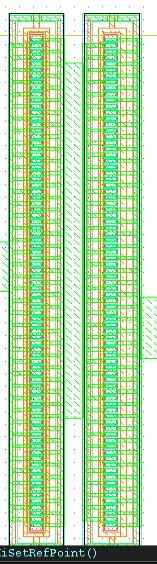
**Layout Description and philosophies behind the layout:**

An initial layout floorplan was developed such that the bond pads were placed at the periphery and the components were placed such that the overall area resembled a square.

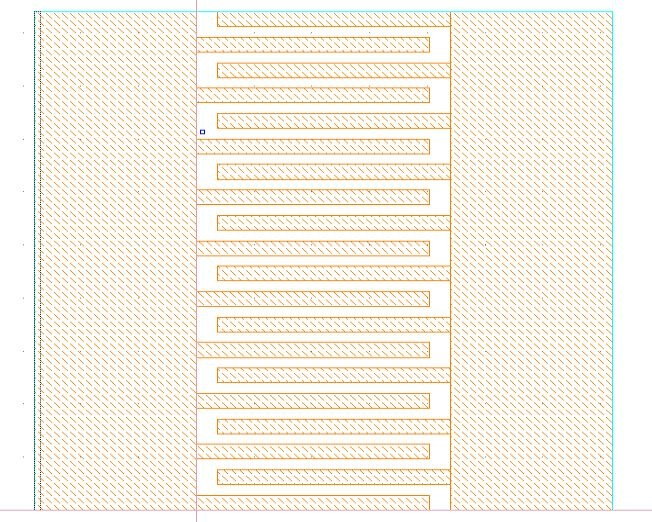
Our design requires 3 on chip inductors and 3 on chip capacitors. The on chip inductors chosen were “ind” from the cmosrf8f library. These inductors have a pattern ground shield in the M1 layer which reduces the substrate resistance and offers a high QL, which we calculated to be around 11.7.



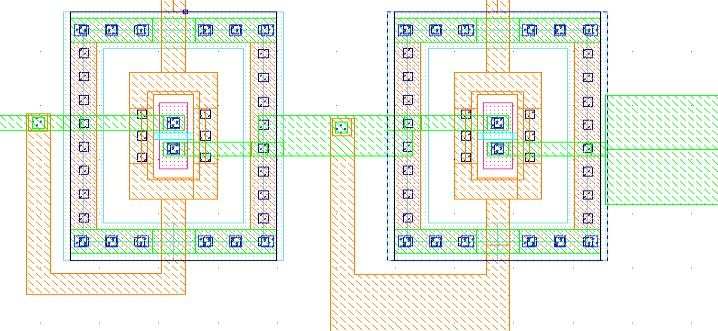
Cascode transistors are laid out in the interdigitated style so that the drain-bulk / source-bulk junction capacitance is minimized. This prevents signal leakage due to parasitics in the high frequency operation. The number of fingers is kept to be 80 so that the gate and source/drain resistances are reduced. In addition, the routing is done so that the overall resistance associated with wires is reduced.



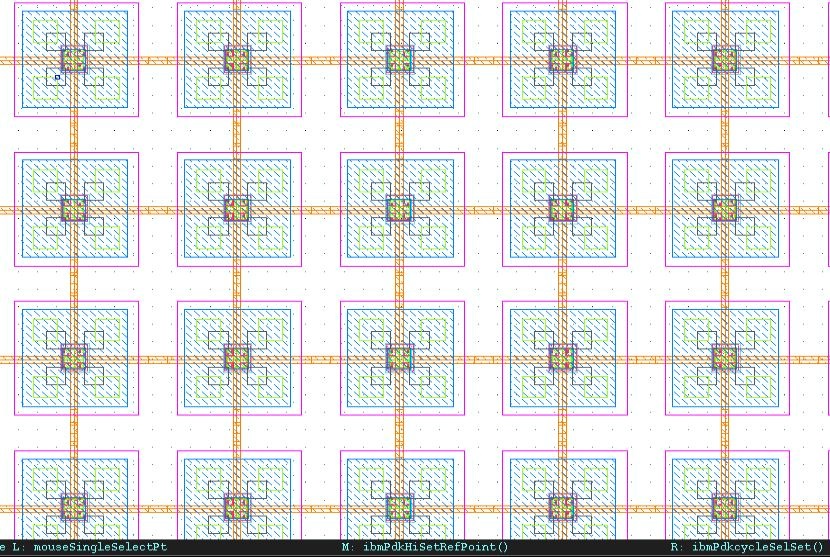
For realizing the capacitances, we make use of “vncap”, which is a metal-oxide-metal capacitance. A better capacitance can be expected with this cap and it makes the layout compact in terms of area. The component we choose is vncap with a ground plane to reduce the parasitic resistance.



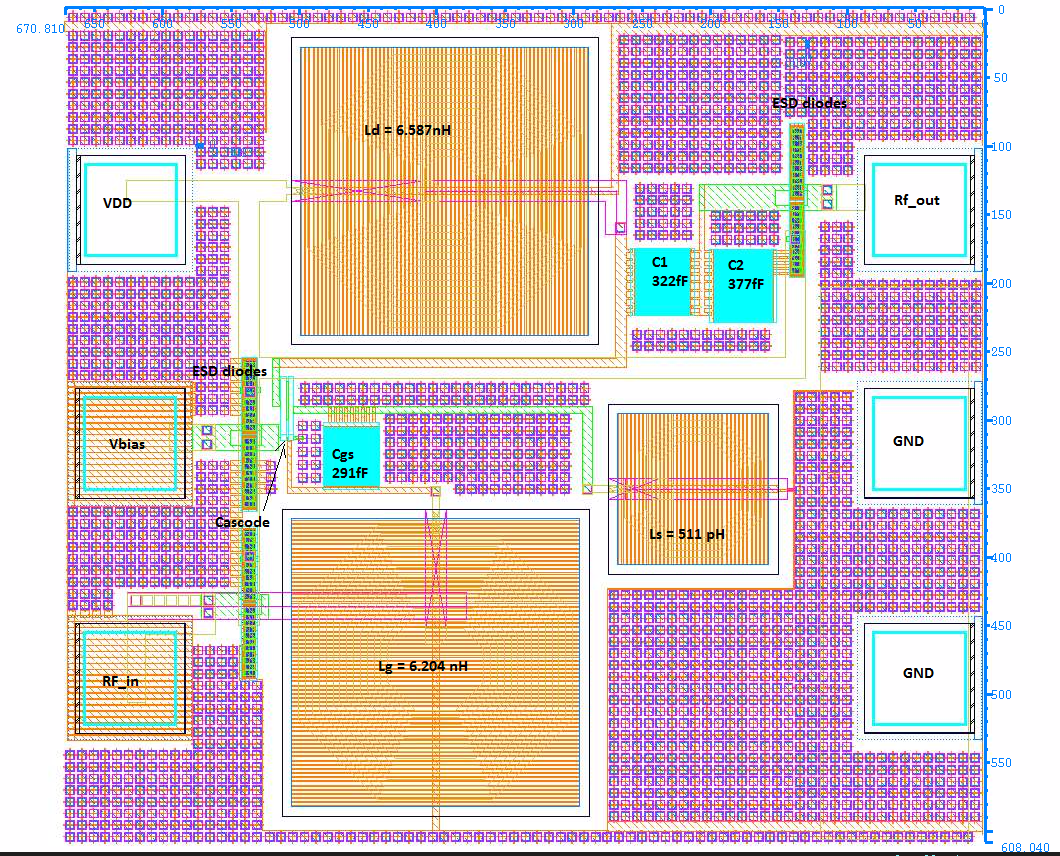
Biasing consists of two Nmos devices which are connected to form a diode.



Since the ground connection is very essential in RF layouts, we created a special ground cell that provided ground connection from top level metal to the substrate. The empty areas in the chip were filled using the ground cell. This also made it easy to make ground connections for all the required components.



**Full Layout**

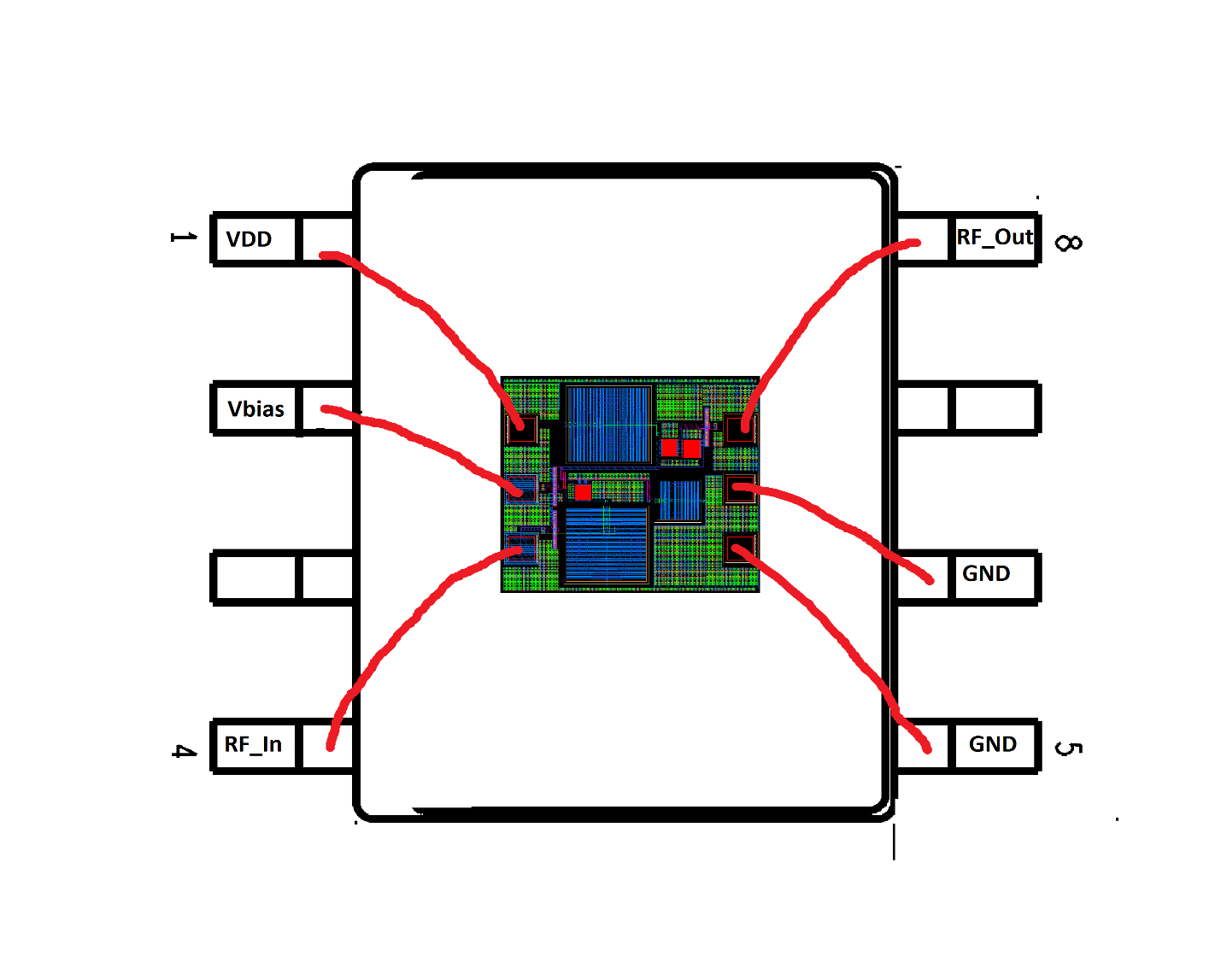
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The overall area is 0.63918mm X 0.72007mm = 0.4602 mm2

This is very close to our initial area estimate. The aspect ratio of the chip is 0.72007/0.63918 = 1.12.

This being close to 1, is a good aspect ratio.

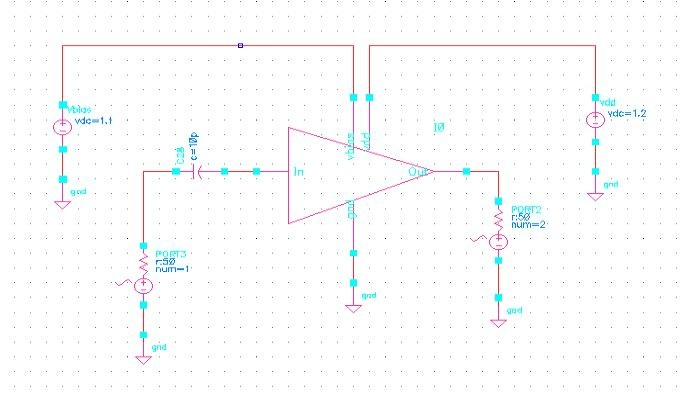
**Bonding diagram of the IC.**



**Instructions for how the circuit should be used.**

Our circuit is highly integrated and requires only 1 external capacitor at the input. The voltages and components required are as follows:

* Bias voltage of 1.1 V
* Supply voltage VDD which can be of the range 1.1 V – 1.3V
* Ground connection GND
* External capacitor of value 10pF to be used at the input pin

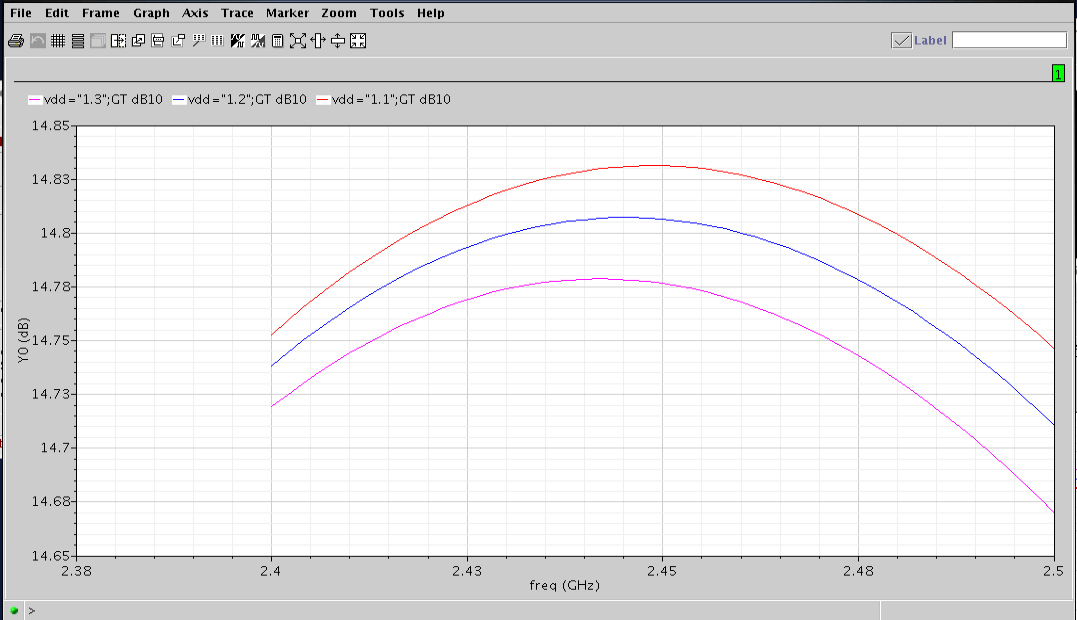
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**Parasitic Extraction/Estimation**

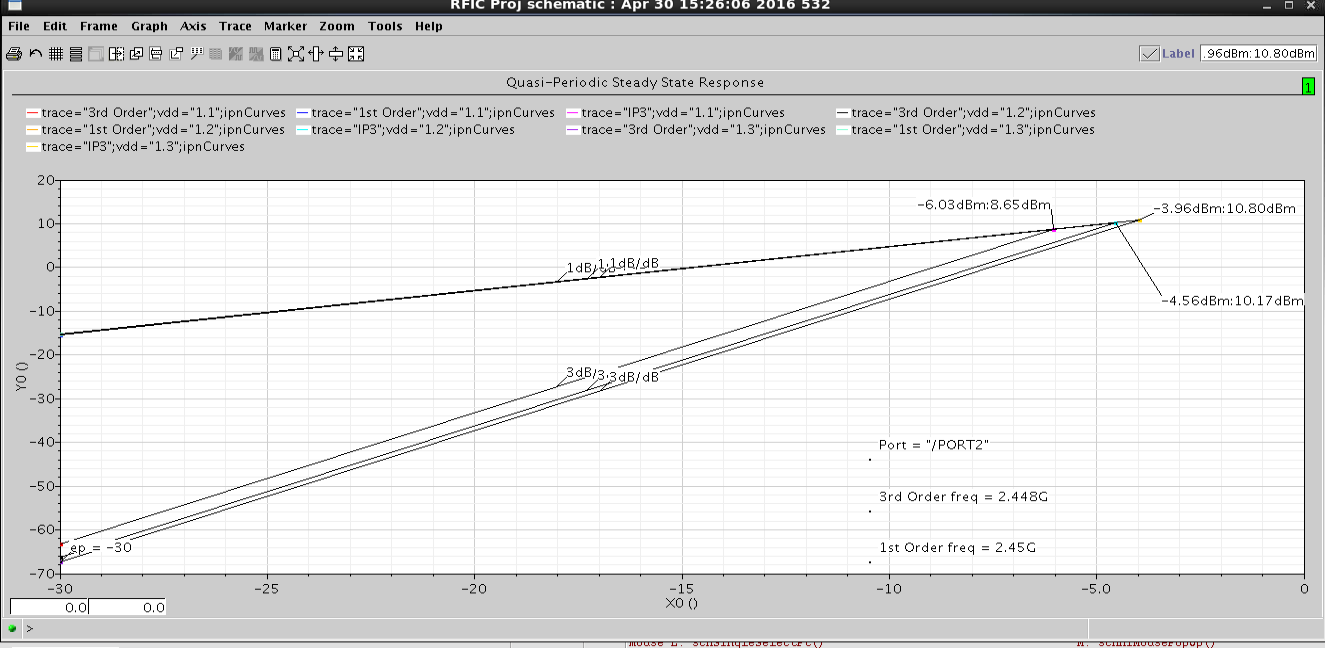
%parasitic capacitances  
Eo=8.85e-12;  
Er=3.9;tox=3.12e-9;  
Cgdl=330e-12;  
Cgsl=330e-12;  
dlc=18e-9;  
pb=0.6;mj=0.5;  
Cj=1e-8;Cjs=2e-12;  
Cgbo=17.06e-12;  
L=120e-9;Lov=1.4e-8;W=72.8e-9;Nf=80;Vj=(-1.093);  
Area=80\*72.8e-9\*6e-10;  
peri=(2\*6e-10)+72.8e-9;  
Cox=abs((Eo\*Er)/tox);  
Cgso=abs((Cox\*dlc)-Cgsl);  
Cgdo=abs((Cox\*dlc)-Cgdl);  
Cgs=abs(((2/3)\*Cox\*W\*(L-2\*Lov))+(Cgso\*W)+(Nf\*Cgbo\*L));  
Cgd=abs(Cgdo\*W);  
Cdb=((Area\*Cj)/(1-(Vj/pb))^mj)+(((peri)\*Cjs)/((1-(Vj/pb))^mj))+((W\*Cjs)/((1-(Vj/pb))^mj));  
x=[Cox Cgso Cgdo Cgs Cgd Cdb];  
disp(x);

Cox=0.011 Cgso=1.39e-10 Cgdo=1.39e-10 Cgs=2.2270e-16 Cgd=9.5277e-18 Cdb=1.7481e-19  
**Circuit Simulation Results**

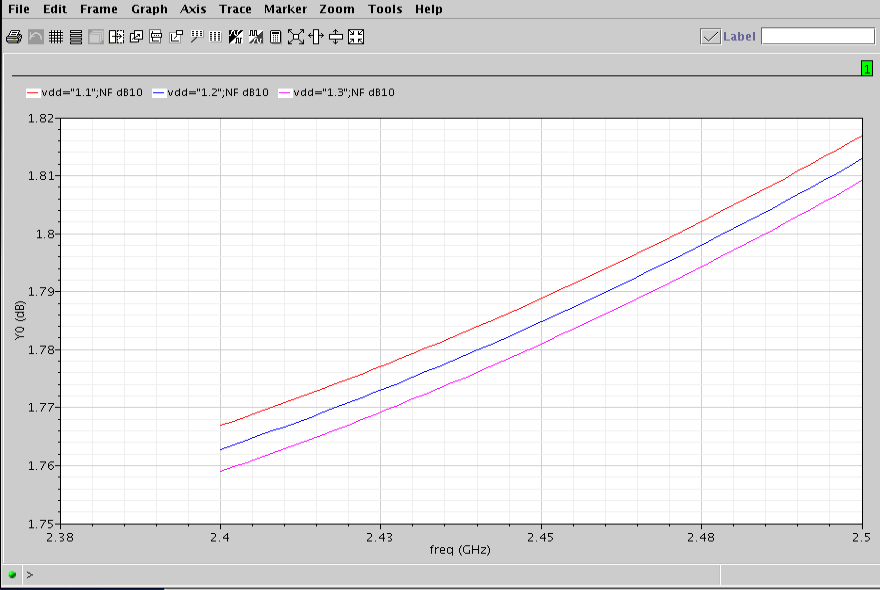
**Transducer Gain(GT)**



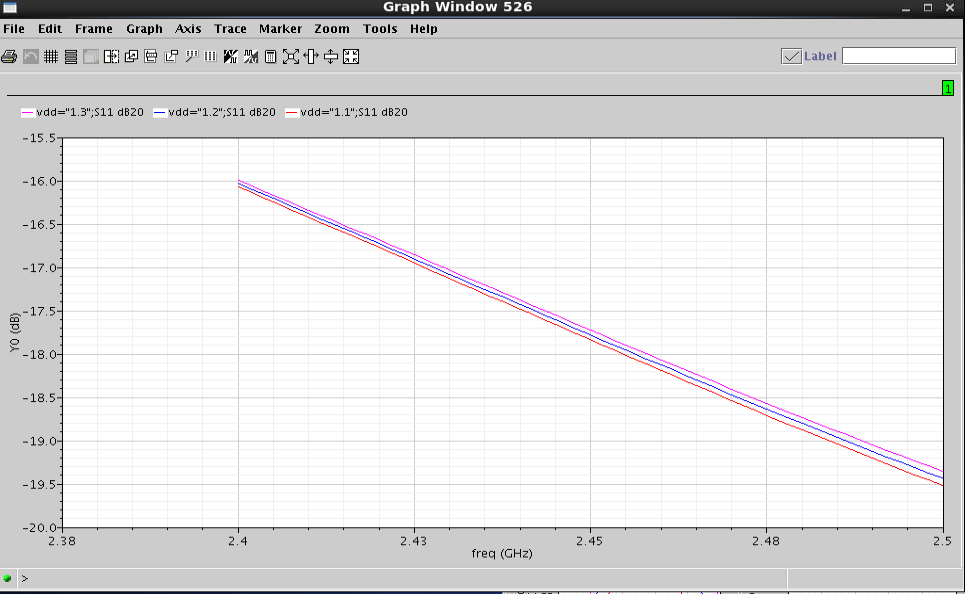
**IIP3 Simulation**



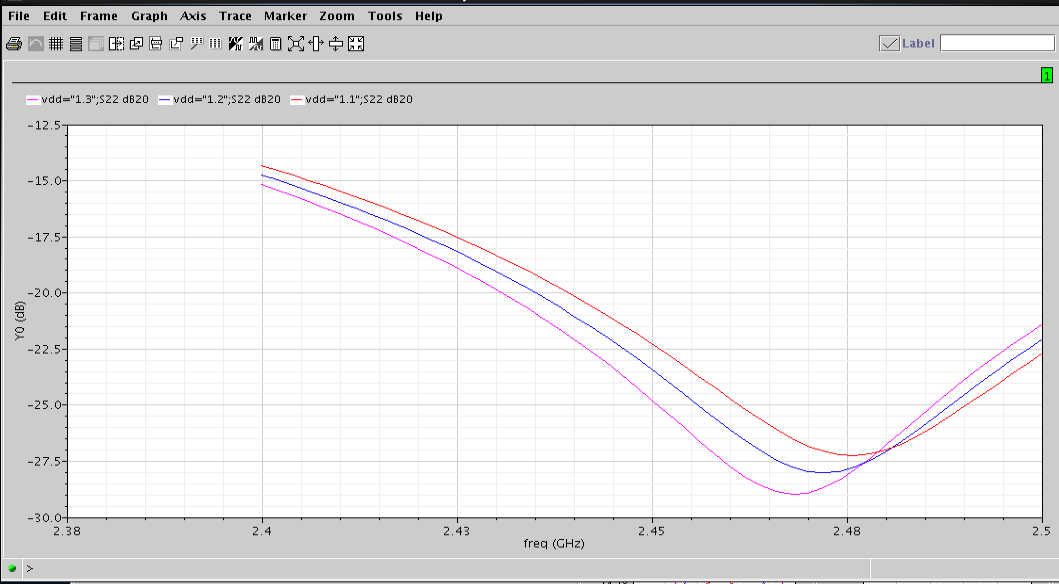
**Noise Factor**



**S11**

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**S22**



**Comparison between Hand/Matlab Analyses and Simulation Results**

|  |  |  |
| --- | --- | --- |
| Specifictions | Hand analysis value at 2.45GHz | Simulation value at 2.45GHz |
| GT | 19.73db | 14.806 db |
| S11 | - ∞ db | -17.06 db |
| S22 | - ∞ db | -23.41 db |
| NF | <2db | 1.78db |
| IIP3 | <-7db | -4.56db |

The variations arise due to the fact that the initial hand analysis did not include the bondpad parasitics, and the values obtained for the components had to be modified to achieve matching at input and output.

**Variability analysis**

We conduct a variability analysis with the following variations:

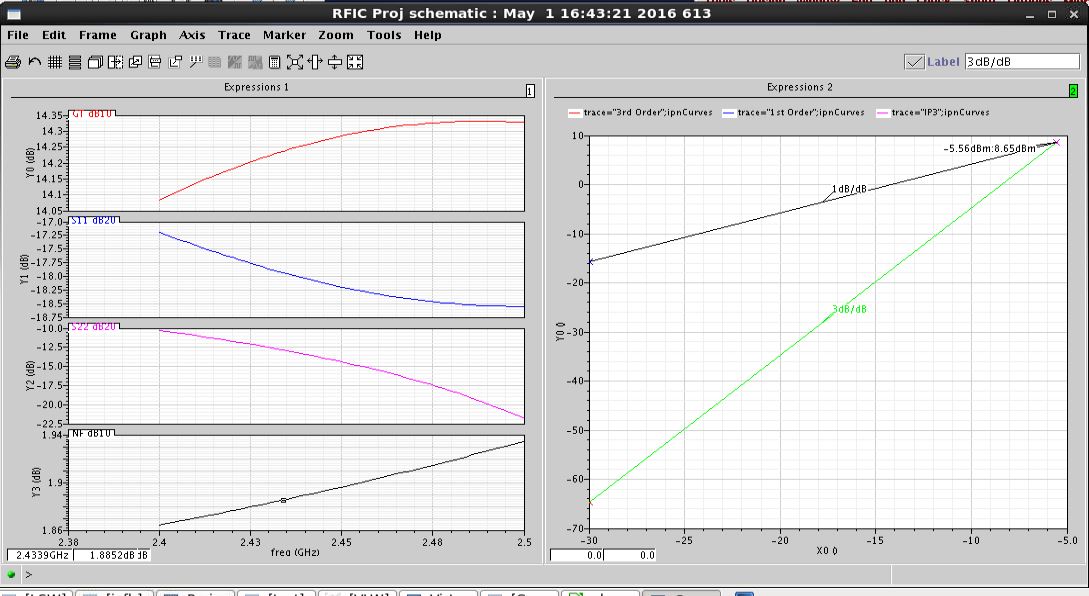
* +/- 3% for on chip inductors
* +/- 10% for on chip capacitors (including transistor capacitance)
* +/- 10% for on external components – which includes a single off chip capacitor

The values for nom and worst case are tabulated below:

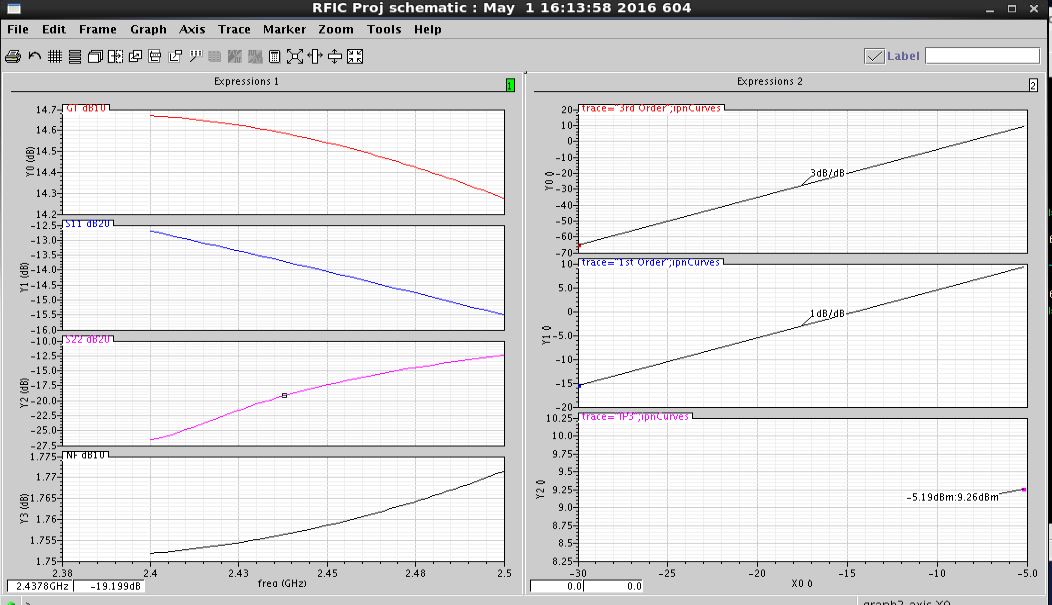
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Component** | **NOM** | **MAX** | **MIN** | **units** |
| Lg | 6.204 | 6.39012 | 6.01788 | nH |
| Ls | 511 | 526.33 | 495.67 | pH |
| Ld | 6.587 | 6.78461 | 6.38939 | nH |
| Cext | 10 | 11 | 9 | pF |
| Cgs | 291 | 320.1 | 261.9 | fF |
| C1(Series cap) | 322 | 354.2 | 289.8 | fF |
| C2 (Shunt Cap) | 377 | 414.7 | 339.3 | fF |
| M1 cap (width) | 72.8 | 80.08 | 65.52 | um |
| M2 cap (width) | 72.8 | 80.08 | 65.52 | um |

In order to test the robustness of the circuit, we applied the extreme values of the components in the opposite directions at the input and output.

**Results with input components varied by +10% and output components varied by -10%**

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**Results with input components varied by -10% and output components varied by +10%**

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As we see from plots, the specifications are met with the worst case

**Conclusion/Summary.**

We have designed a low noise amplifier to meet the required specifications. The circuit is highly integrated and requires a single external component. The circuit is biased for an Id of 1.7mA. The power consumption at 1.2V is around 2.04mW, hence this is a low power circuit.

The layout has been designed to optimize area and reduce parasitics. The components are chosen with a pattern shield to minimize parasitic resistance. In addition, special ground cells have been added to ensure proper grounding to the substrate.